REMARKS

Claims 1-3, 5-7, 9-11, 13-19, 21-26, 28-32 and 34-36 remain pending in the Application. No new matter has been added. Applicants respectfully request reconsideration in view of the following remarks.

I. Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1-3, 5-7, 9-11, 13-19, 21-26, 28-32 and 34-36 as allegedly unpatentable over U.S. Patent No. 6,738,248 (hereinafter referred to as "Jenkins") in view of U.S. Patent No. 5,994,760 (hereinafter referred to as "Duclos"). Applicants respectfully traverse this rejection.

a. Claim 1 and its dependent claims

Claim 1 is directed to a low noise amplifier that includes a radio frequency input and an electrostatic discharge ("ESD") protection circuit to shunt ESD current during positive and negative ESD events away from the radio frequency input and through a first supply. The ESD protection circuit includes a pair of diodes and a separate ESD clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event. The first diode of the pair has a first terminal coupled to the radio frequency input and a second terminal directly coupled to a first supply. The second diode of the pair has a second terminal coupled to the radio frequency input and a first terminal directly coupled to the first supply.

The Examiner suggests that Jenkins' input-output pad 104 is Applicants' claimed radio frequency input and that Jenkins' protection circuit 108 is Applicants' claimed electrostatic discharge protection circuit. The Examiner acknowledges that Jenkins does not teach Applicants' claimed separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event. However, the Examiner suggests that Fig. 2 of Duclos shows an ESD clamp. The Examiner further suggests that it would have been obvious to incorporate Duclos' clamp into Jenkins' design "for the purpose of protecting the buffer (102) from ESD occurring from the power supply." Applicants respectfully disagree.

Jenkins shows a protection circuit that protects the internal devices of a differential input buffer 102 during ESD events. (Col. 3, lines 6-10). The differential input buffer 102 transmits and receives data over differential transmission media, such as two-wire transmission lines, through input-output pads 104 and 106. (Col. 2, lines 37-43; Fig. 2). The protection circuit includes two back-to-back diode pairs coupled between the inputs to the buffer and a voltage supply VSS. (Col. 3, lines 16-20). In response to an ESD event, one or more of the diodes turns on and discharges the ESD current directly to the VSS supply rails. (Col. 3, lines 43-53).

Applicants respectfully assert that Jenkins fails to teach or suggest, at least, a radio frequency input. The Examiner suggests that Jenkins' input-output pad 104 is Applicants' claimed radio frequency input. However, Jenkins' input-output pads 104 and 106 do not receive radio frequency signals, i.e., electromagnetic waves that are transmitted through free space. Rather, the input-output pads receive differential signals sent over two-wire transmission lines. (Col. 2, lines 38-43). Therefore, Jenkins does not teach or suggest Applicants' claimed radio frequency input. Applicants respectfully assert that claim 1 is allowable for at least this reason.

Additionally, Applicants respectfully assert that the combination of Jenkins and Duclos is improper. The Examiner suggests that it would have been obvious to incorporate Duclos' ESD clamp "between the terminals VDD and VSS of Jenkins et al., for the purpose of protecting the buffer (102) from ESD occurring from the power supply." However, Jenkins already provides a way to protect the buffer from ESD occurring from the power supply. In particular, Jenkins shows that a direct path exists between supplies VDD and VSS for discharging ESD events occurring at either supply. (Fig. 3). Power supplies VDD and VSS are directly coupled to each other through diodes D5 and D6. (Col. 4, lines 42-45). The input to buffer 102 is coupled to the node between diodes D5 and D6 through the protection circuit 108. (Col. 4, lines 35-39). Therefore, diodes D5 and D6 provide a discharge path to the supply rails for ESD events occurring at any of VDD, VSS, and the input. (Col. 4, lines 39-41). Applicants respectfully point out that because Jenkins already discloses a way to protect the input buffer from ESD occurring at the power supplies, it would be redundant to include a secondary method of protection, i.e., to incorporate the ESD clamp of Duclos. Therefore, Applicants respectfully assert that claim 1 is allowable for at least this reason.

The Examiner suggests that it would have been obvious to incorporate the ESD clamp of Duclos between the terminals VDD and VSS of Jenkins. This suggestion ignores the fact that Jenkins' design *already includes* an ESD clamp, the protection circuit 108. (Fig. 3). Not only did Jenkins know about ESD clamps at the time of his design, he actually used one to protect the input buffer, as shown in Fig. 3 of Jenkins. However, this configuration differs from Applicants' claimed clamp directly coupled between a high voltage supply and a low voltage supply, as the Examiner acknowledged by withdrawing the 35 U.S.C. § 102 rejection based solely on Jenkins in the previous Action. Applicants respectfully assert that the Examiner has not established a motivation to combine the teachings of Jenkins and Duclos, and claim 1 is allowable for this additional reason.

Claims 2-3 and 5-8 depend from claim 1, and are allowable for at least the same reasons set forth above with respect to claim 1.

Claim 5 is also separately allowable for at least the following additional reason. Claim 5 recites that the positive and negative electrostatic discharge events include a radio frequency input to high voltage supply positive discharge pulse, a radio frequency input to high voltage supply negative discharge pulse, a radio frequency input to low voltage supply positive discharge pulse, and a radio frequency input to low voltage supply negative discharge pulse. The Examiner suggests that Jenkins' ESD events "necessarily include" Applicants' claimed radio frequency input to supply pulses. However, as discussed above, Jenkins' protection circuit does not accept a radio frequency input; rather, Jenkins' circuit receives differential input signals that are transmitted over *transmission lines*. Therefore, Jenkins' ESD events do not necessarily include the discharge events as recited in claim 5. Applicants respectfully assert that claim 5 is allowable for at least this additional reason.

Claim 6 is also separately allowable for at least the following additional reason. Claim 6 recites that the low voltage supply floats during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse. The Examiner suggests that Fig. 3 of Jenkins shows Applicants' claimed floating low voltage supply. However, Jenkins' low voltage supply VSS does not float during a high voltage supply discharge pulse; rather, VSS is the final point of discharge for high supply ESD current, and is consequently maintained at a constant level. (Col. 4, lines 39-45). Indeed, Jenkins'

protection circuit will not operate correctly if VSS is allowed to float. For example, if VSS floats during a high voltage supply discharge pulse (i.e., to a level above two diode-drops of VDD), diode D6 will not conduct, and the ESD current will be discharged into buffer 102. Therefore, Applicants respectfully assert that claim 6 is allowable for at least this additional reason.

Claim 7 is also separately allowable for at least the following additional reason. Claim 7 recites that the high voltage supply floats during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse. The Examiner suggests that Fig. 3 of Jenkins shows Applicants' claimed floating high voltage supply. However, Jenkins' high voltage supply VDD is the final point of discharge for low supply ESD current and must be maintained at a constant level for reasons similar to those given above with respect to claim 6. (Col. 4, lines 39-45). Therefore, Applicants respectfully assert that claim 7 is allowable for at least this additional reason.

Claim 8 is also separately allowable for at least the following additional reason. Claim 8 recites that the low noise amplifier is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, and 802.11i, and 802.14. The Examiner suggests that it would be "obvious... that a device used in a high speed communication circuit would necessarily be compliant by IEEE standards." However, IEEE standard 802.11 applies to wireless local area network specifications. As discussed above, Jenkins' circuit relates to differential signals transmitted over transmission lines. Jenkins' design would not "necessarily be compliant" with IEEE standards relating to *wireless networks*, because these wireless standards would be irrelevant to designing a device relating to data transmitted and received over transmission lines. Therefore, Applicants respectfully assert that claim 8 is allowable for at least this additional reason.

b. Claim 9 and its dependent claims

Claim 9 is directed to a low noise amplifier that includes receiving means for receiving an RF input and shunting means to shunt ESD current during positive and negative ESD events away from the receiving means and through a first supply. The shunting means includes a pair of diode means and a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event.

The first diode means of the pair has a first terminal coupled to the receiving means and a second terminal directly coupled to a first supply. The second diode means of the pair has a second terminal coupled to the receiving means and a first terminal directly coupled to the first supply.

Claim 9 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 10-11 and 13-17 depend from claim 9 and are allowable for at least the same reasons set forth above with respect to claim 9.

Claim 13 is also separately allowable for at least the same reasons set forth above with respect to claim 5.

Claim 14 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 15 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

Claim 16 is also separately allowable for at least the same reasons set forth above with respect to claim 8.

c. Claim 17 and its dependent claims

Claim 17 is directed to an ESD protection circuit to shunt ESD current during positive and negative ESD events. The protection circuit includes a pair of diodes and a separate ESD clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event. The first diode of the pair has a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply. The second diode of the pair has a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply.

Claim 17 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 18-19 and 21-23 depend from claim 17 and are allowable for at least the same reasons set forth above with respect to claim 17.

Claim 21 is also separately allowable for at least the same reasons set forth above with respect to claim 5.

Claim 22 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 23 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

d. Claim 24 and its dependent claims

Claim 24 is directed to an ESD protection circuit that includes shunting means for shunting ESD current during positive and negative ESD events and a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event. The shunting means includes a pair of diode means. The first diode means of the pair has a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply. The second diode means of the pair has a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply.

Claim 24 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 25-26 and 28-30 depend from claim 24 and are allowable for at least the same reasons set forth above with respect to claim 24.

Claim 28 is also separately allowable for at least the same reasons set forth above with respect to claim 5.

Claim 29 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 30 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

e. Claim 31 and its dependent claims

Claim 31 is directed to a method for discharging ESD that includes providing a first direct discharge path between an input/output pad and a first supply, providing a second direct discharge path between the input/output pad and the first supply, providing a third discharge path between the first supply and a second supply during an ESD event; and shunting ESD current during positive and negative ESD events through one of the first discharge path and the second discharge path.

The Examiner acknowledges that Jenkins does not teach Applicants' claimed providing a third discharge path between the first supply and a second supply during an electrostatic

discharge event. The Examiner suggests that Duclos teaches an ESD clamp directly coupled between high and low voltage supplies. The Examiner further suggests that it would have been obvious to incorporate Duclos' ESD clamp into Jenkins' design "for the purpose of protecting the buffer (102) from ESD occurring from the power supply." However, as discussed above, Jenkins already provides a discharge path to protect the input buffer from ESD occurring at the power supplies. It would be redundant to include a secondary method of protection, i.e., to incorporate the ESD clamp of Duclos. Therefore, Applicants respectfully assert that claim 31 is allowable for at least this reason.

Claims 32 and 34-36 depend from claim 31 and are allowable for at least the same reasons set forth above with respect to claim 31.

Claim 34 is also separately allowable for at least the same reasons set forth above with respect to claim 5.

Claim 35 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 36 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

II. Conclusion

No fees are believed to be due at this time. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 2-6-07

42,596

For Mark D. Kirkland
Reg. No. 40,048

CUSTOMER NO. 26200
Fish & Richardson P.C.
500 Arguello Street, Suite 500
Redwood City, California 94063
Telephone: (650) 839-5070
Facsimile: (650) 839-5071